WHAT IS CLAIMED IS:

1 A nickel silicide film formation method, comprising steps of:

a step for forming a layer structure containing silicon and nickel on a substrate at a first substrate temperature which does not cause a silicide reaction; and

a step of the silicide reaction for forming nickel monosilicide by implementing a thermal treatment of the layer structure at a second substrate temperature which causes a nickel monosilicide reaction,

wherein, in the step for forming the layer structure, a ratio (N_{Ni}/N_{si}) of a number of total nickel atoms (N_{Ni}) to a number of total silicon atoms (N_{si}) existing in a whole layer structure is equal to or more than 1.

2 A nickel silicide film formation method according to claim 1, wherein the step for forming the layer structure is consist of co-depositing step of nickel and silicon.

3 A nickel silicide film formation method according to claim 1, wherein the step for forming the layer structure is consist of a step alternately forming at least one nickel layer and at least one silicon layer.

4 A nickel silicide film formation method according to claim 3, wherein the layer structure is formed such that a ratio of the number of nickel atoms in each nickel layer contained in the layer structure to the number of silicon atoms in each silicon layer contained in the layer structure is equal to a ratio of the number of total nickel atoms to the number of total silicon atoms existing in a whole layer structure.

5 A nickel silicide film formation method according to claim 1, wherein the ratio (N_{Ni}/N_{si}) of the number of total nickel atoms (N_{Ni}) to the number of total silicon atoms (N_{si}) existing in the whole layer structure is equal to or more than 1, and equal to or less than 4.

6 A nickel silicide film formation method according to claim 1, wherein

the nickel silicide contains the nickel monosilicide equal to or more than 50 %.

7 A nickel silicide film formation method according to claim 1, wherein a region of at least one semiconductor selected from a group of single crystal silicon, poly crystal silicon, distorted silicon, single crystal silicon-germanium, poly crystal silicon-germanium, and distorted silicon-germanium is included in an uppermost surface of the substrate

8 A nickel silicide film formation method according to claim 1, wherein the substrate is any one selected from a group of a silicon substrate, a SOI substrate, and a SGOI substrate.

9 A nickel silicide film formation method according to claim 1, wherein the layer structure formed with the step of forming the layer structure is an amorphous state.

10 A nickel silicide film formation method according to claim 3, wherein each thickness of the silicon layer and the nickel layer formed with the step of forming the layer structure is in a range of 2 nm - 10 nm.

11 A nickel silicide film formation method according to claim 1, wherein a surface orientation of a principal surface of the substrate is other than (111) surface.

12 A nickel silicide film formation method according to claim 1, further comprising a step of:

a step for implementing a preliminary thermal treatment at a low temperature lower than the second substrate temperature after the step of forming the layer structure and before the step of the silicide reaction.

13 An etching method for etching a nickel-rich region located on an insulator region of a nickel silicide film which is formed on at least one semiconductor region and at least one insulator region on a substrate and a

composition of the nickel silicide film is different between the semiconductor region and the insulator region,

wherein a ratio (N_{Ni}/N_{si}) of a number of nickel atoms (N_{Ni}) to a number of silicon atoms (N_{si}) in the nickel-rich region is equal to or more than 1.11.

14 An etching method according to claim 13, wherein a region of the nickel silicide film located on the semiconductor region is composed of nickel monosilicide and a region of the nickel silicide film located on the insulator region is composed of nickel-rich nickel silicide.

15 An etching method according to claim 13, wherein the semiconductor region comprises at least one semiconductor selected from a group of single crystal silicon, poly crystal silicon, distorted silicon, single crystal silicon-germanium, poly crystal silicon-germanium, and distorted silicon-germanium.

16 An etching method according to claim 13, wherein the insulator region comprises at least one selected from silicon oxide and silicon nitride.

17 An etching method according to claim 13, wherein the nickel silicide film is formed with a step for forming a stacked layer film by alternately forming at least one nickel layer and at least one silicon layer at a first substrate temperature which does not cause a silicide reaction, and a step of the silicide reaction for implementing a thermal treatment of the stacked layer film at a second substrate temperature which causes a nickel monosilicide reaction.

18 An etching method according to claim 17, wherein the silicon layer formed with the step for forming the stacked layer film is an amorphous state.

19 An etching method according to claim 17, wherein each thickness of the silicon layer and the nickel layer formed with the step for forming the stacked layer film is in a range of 2 nm – 10 nm.

20 An etching method according to claim 13, wherein the nickel silicide film is formed with a step for co-depositing nickel and silicon, and a step of a silicide reaction for implementing a thermal treatment at a second substrate temperature which causes a nickel monosilicide reaction.

21 An etching method according to claim 13, wherein the substrate is any one selected from a group of a silicon substrate, a SOI substrate, and a SGOI substrate.

22 An etching method according to claim 13, wherein a surface orientation of a principal surface of the substrate is other than (111) surface.

23 An etching method for etching a nickel-rich region located on an insulator region of a nickel silicide film which is formed on at least one semiconductor region and at least one insulator region on a substrate and a composition of the nickel silicide film is different between the semiconductor region and the insulator region,
wherein the nickel-rich region has a diffraction peak of Ni_2Si in X-ray diffraction pattern.

24 An etching method according to claim 23, wherein a region of the nickel silicide film located on the semiconductor region is composed of nickel monosilicide and a region of the nickel silicide film located on the insulator region is composed of nickel-rich nickel silicide.

25 An etching method according to claim 23, wherein the semiconductor region comprises at least one semiconductor selected from a group of single crystal silicon, poly crystal silicon, distorted silicon, single crystal silicon-germanium, poly crystal silicon-germanium, and distorted silicon-germanium.

26 An etching method according to claim 23, wherein the insulator region comprises at least one selected from silicon oxide and silicon nitride.

27 An etching method according to claim 23, wherein the nickel silicide film is formed with a step for forming a stacked layer film by alternately forming at least one nickel layer and at least one silicon layer at a first substrate temperature which does not cause a silicide reaction, and a step of the silicide reaction for implementing a thermal treatment of the stacked layer film at a second substrate temperature which causes a nickel monosilicide reaction.

28 An etching method according to claim 27, wherein the silicon layer formed with the step for forming the stacked layer film is an amorphous state.

29 An etching method according to claim 27, wherein each thickness of the silicon layer and the nickel layer formed with the step for forming the stacked layer film is in a range of 2 nm – 10 nm.

30 An etching method according to claim 23, wherein the nickel silicide film is formed with a step for co-depositing nickel and silicon, and a step of a silicide reaction for implementing a thermal treatment at a second substrate temperature which causes a nickel monosilicide reaction.

31 An etching method according to claim 23, wherein the substrate is any one selected from a group of a silicon substrate, a SOI substrate, and a SGOI substrate.

32 An etching method according to claim 23, wherein a surface orientation of a principal surface of the substrate is other than (111) surface.

33 A semiconductor device fabrication method, comprising steps of:

a step for forming a layer structure containing silicon and nickel on at least one semiconductor region and on at least one insulator region on a substrate at a first substrate temperature which does not cause a silicide reaction; and

a step of the silicide reaction for forming a nickel silicide film containing nickel monosilicide, of which composition is different on the semiconductor region and on the insulator region, by implementing a thermal treatment of the layer structure at a second substrate temperature which causes a nickel monosilicide reaction,

wherein, in the step for forming the layer structure, a ratio (N_{Ni}/N_{Si}) of a number of total nickel atoms (N_{Ni}) to a number of total silicon atoms (N_{Si}) existing in a whole layer structure is equal to or more than 1.

34 A semiconductor device fabrication method according to claim 33, wherein nickel silicide located on the semiconductor region after the silicide reaction step is composed of nickel monosilicide and the nickel silicide located on the insulator region after the silicide reaction step is composed of nickel-rich nickel silicide.

35 A semiconductor device fabrication method according to claim 33, further comprising a step of:

an etching step for removing the nickel-rich nickel silicide located on the insulator region of the nickel silicide film by etching, thereby forming the nickel silicide film only on the semiconductor region with a self-aligning manner.

36 A semiconductor device fabrication method according to claim 33, wherein the step for forming the layer structure is consist of co-depositing step of nickel and silicon.

37 A semiconductor device fabrication method according to claim 33, wherein the step for forming the layer structure is consist of alternately forming at least one nickel layer and at least one silicon layer.

38 A semiconductor device fabrication method according to claim 33, wherein the semiconductor region comprises at least one semiconductor selected from a group of single crystal silicon, poly crystal silicon, distorted silicon, single crystal silicon-germanium, poly crystal silicon-germanium,

and distorted silicon-germanium.

39 A semiconductor device fabrication method according to claim 33, wherein the insulator region comprises at least one selected from silicon oxide and silicon nitride.

40 A semiconductor device fabrication method according to claim 33, wherein the substrate is any one selected from a group of a silicon substrate, a SOI substrate, and a SGOI substrate.

41 A semiconductor device fabrication method according to claim 33, wherein the layer structure formed with the step for forming the layer structure is an amorphous state.

42 A semiconductor device fabrication method according to claim 37, wherein each thickness of the silicon layer and the nickel layer formed with the step for forming the layer structure is in a range of 2 nm - 10 nm.

43 A semiconductor device fabrication method according to claim 33, wherein a surface orientation of a principal surface of the substrate is other than (111) surface.

44 A semiconductor device fabrication method according to claim 33, further comprising a step of:

a step for implementing a preliminary thermal treatment at a low temperature lower than the second substrate temperature after the step for forming the layer structure and before the step of the silicide reaction.

45 A semiconductor device fabrication method according to claim 44, further comprising a step of:

an etching step for etching off only a region closer to an amorphous state having a poor crystallity located on the insulator region of the layer structure before the silicide reaction step and after the preliminary thermal treatment, thereby forming the nickel silicide film only on the

semiconductor region with a self-aligning manner by implementing the silicide reaction only for a remained region on the semiconductor region of the layer structure.

46 A nickel silicide formation method, comprising steps of:

a step for forming a layer structure containing silicon and nickel on at least one semiconductor region and at least one insulator region on a substrate; and

a step of a silicide reaction for forming a nickel silicide film having a nickel monosilicide composition on the semiconductor region as well as having a nickel-rich composition on the insulator region by implementing a thermal treatment of the layer structure at a second substrate temperature which causes a nickel monosilicide reaction,

wherein, in a nickel-rich region located on the insulator region of the nickel silicide film, a ratio (N_{Ni}/N_{si}) of a number of nickel atoms (N_{Ni}) to a number of silicon atoms (N_{si}) is equal to or more than 1.11.

47 A nickel silicide formation method according to claim 46, wherein a region of the nickel silicide film located on the semiconductor region is composed of nickel monosilicide and a region of the nickel silicide film located on the insulator region is composed of nickel-rich nickel silicide.

48 A nickel silicide formation method according to claim 46, wherein the step for forming the layer structure is consist of alternately forming at least one nickel layer and at least one silicon layer at a first substrate temperature which does not cause the silicide reaction.

49 A nickel silicide formation method according to claim 48, wherein the silicon layer formed with the step for forming the layer structure is an amorphous state.

50 A nickel silicide formation method according to claim 46, wherein the step for forming the layer structure is consist of co-depositing step of nickel and silicon.

51 A nickel silicide formation method according to claim 46, further comprising a step of:

a step for implementing a preliminary thermal treatment at a low temperature lower than the second substrate temperature after the step for forming the layer structure and before the step of the silicide reaction.

52 A nickel silicide formation method, comprising steps of:

a step for forming a layer structure containing silicon and nickel on at least one semiconductor region and at least one insulator region on a substrate; and

a step of a silicide reaction for forming a nickel silicide film having a nickel monosilicide composition on the semiconductor region as well as having a nickel-rich composition on the insulator region by implementing a thermal treatment of the layer structure at a second substrate temperature which causes a nickel monosilicide reaction,

wherein a nickel-rich region located on the insulator region of the nickel silicide film has a diffraction peak of Ni_2Si in X-ray diffraction pattern.

53 A nickel silicide formation method according to claim 52, wherein a region of the nickel silicide film located on the semiconductor region is composed of nickel monosilicide and a region of the nickel silicide film located on the insulator region is composed of nickel-rich nickel silicide.

54 A nickel silicide formation method according to claim 52, wherein the step for forming the layer structure is consist of alternately forming at least one nickel layer and at least one silicon layer at a first substrate temperature which does not cause the silicide reaction.

55 A nickel silicide formation method according to claim 54, wherein the silicon layer formed with the step for forming the layer structure is an

amorphous state.

56 A nickel silicide formation method according to claim 52, wherein the step for forming the layer structure is consist of co-depositing step of nickel and silicon.

57 A nickel silicide formation method according to claim 52, further comprising a step of:

a step for implementing a preliminary thermal treatment at a low temperature lower than the second substrate temperature after the step for forming the layer structure and before the step of the silicide reaction.

58 A nickel silicide formation method, comprising steps of:

a step for forming a stacked layer film by alternately forming at least one nickel layer and at least one silicon layer on a substrate at a first substrate temperature which does not cause a silicide reaction; and

a step of the silicide reaction for forming a nickel silicide film by implementing a thermal treatment of the stacked layer film at a second substrate temperature which causes a nickel monosilicide reaction,

wherein, in the step for forming the stacked layer film, a ratio of a total silicon layer thickness to a total nickel layer thickness in the stacked layer film is equal to or less than 1.79.

59 A nickel silicide formation method according to claim 58, wherein the silicon layer formed with the step for forming the stacked layer film is an amorphous state.

60 A semiconductor device fabrication method, comprising steps of:

a step for forming a stacked layer film by alternately forming at least one nickel layer and at least one silicon layer on at least one semiconductor region and on at least one insulator region on a substrate at a first substrate

temperature which does not cause a silicide reaction; and

a step of the silicide reaction for forming a nickel silicide film containing nickel monosilicide, of which composition is different on the semiconductor region and on the insulator region, by implementing a thermal treatment of the stacked layer film at a second substrate temperature which causes nickel monosilicide reaction,

wherein, in the step for forming the stacked layer film, a ratio of a total silicon layer thickness to a total nickel layer thickness in the stacked layer film is equal to or less than 1:79.

61 A semiconductor device fabrication method according to claim 60, further comprising a step of:

an etching step for removing the nickel-rich nickel silicide located on the insulator region of the nickel silicide film by etching, thereby forming the nickel silicide film only on the semiconductor region with a self-aligning manner.

62 A semiconductor device fabrication method according to claim 60, wherein the silicon layer formed with the step for forming the stacked layer film is an amorphous state.

63 A semiconductor device fabrication method, comprising steps of:

a step for forming a layer structure containing silicon and nickel on at least one semiconductor region and at least one insulator region on a substrate at a first substrate temperature which does not cause a silicide reaction;

a step for forming a region having a low crystallity close to an amorphous state located on the insulator region and a region having a high crystallity located on the semiconductor region by implementing a preliminary thermal treatment at a temperature lower than a second substrate temperature;

a step of etching for removing only the region having the low

crystallity close to the amorphous state located on the insulator region; and

a step of the silicide reaction for forming a nickel silicide film with a self-aligning manner only on the semiconductor region by implementing a thermal treatment for the high crystallity region remained on the semiconductor region at the second substrate temperature which causes a nickel monosilicide reaction,

wherein, in the step for forming the layer structure, a ratio (N_{Ni}/N_{si}) of a number of total nickel atoms (N_{Ni}) to a number of total silicon atoms (N_{si}) existing in a whole layer structure is equal to or more than 1.

64 A semiconductor device fabrication method according to claim 63, wherein the step for forming the layer structure is consist of alternately forming at least one nickel layer and at least one silicon layer at the first substrate temperature which does not cause the silicide reaction.

65 A semiconductor device fabrication method according to claim 63, wherein the step for forming the layer structure is consist of co-depositing step of nickel and silicon.